REMARKS

Claims 1 through 25 are pending in this application.

I. CLAIM REJECTIONS - 35 U.S.C. § 102

Claims 1-3, 5-18 and 22-25 are rejected under 35 U.S.C. §102 (b) as being anticipated by Bassetti et al. (5,757,338). The Applicant respectfully traverses.

No claim is anticipated under 35 U.S.C. §102 (b) unless all of the elements are found in exactly the same situation and united in the same way in a single prior art reference. As mentioned in the **MPEP §2131**, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Every element must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). The identical invention must be shown in as complete detail as is contained in the patent claim. *Id.*, "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970), and MPEP 2143.03.

The Examiner states that as to claims 1-3, 5-18 and 22-25, Bassetti et al. teaches a computer system comprising an LCD display (22); a clock generator (a clock generator in PC) (see figures 6-7; column 5, lines 24-29 and column 2, lines 30-33); a graphic processing unit (72, 52, 54, 56, 60) for

converting an image signal provided from at least one of the CPU and a memory (50) into a signal displayed on the LCD (22) and a spread spectrum unit (74) provided between the graphic processing unit (72, 52, 54, 56, 60, 62) and the LCD (22) for modulating a frequency of the clock signal from the clock generator within a predetermined frequency range (see figures 7-12, 15; column 2, lines 30-33; column 7, lines 2-8; column 8, lines 52-68; column 9; column 16, lines 10-68 and column 17, lines 1-41).

However, if for arguments sake only, the Applicant were to assume that graphic processing unit is 72, 52, 54, 56, 60, 62 (mentioned by examiner in line 15, page 2 of paper number 4), the spread spectrum unit is reference 74 and the LCD is reference 22 of Bassetti as the Examiner explains, then as seen in figure 7, the spread spectrum unit 74 is not provided between the graphic processing unit and the LCD 22. As seen in figure 7, the output of reference 74 goes into the parts of the EMI FIFO 60 and LCD controller 62 and then from the LCD controller 62 the signal goes into the LCD. Therefore, clearly as seen in the signal path, modulated clock 74 (spread spectrum unit according to the Examiner) is *not* in between the graphic processing unit (72, 52, 54, 56, 60, 62 according to the Examiner on page 2 of paper number 4) and the LCD (22 in figure 7). On the other hand, in the present invention, the spread spectrum unit is between the graphic processing unit and the LCD. As mentioned above, the identical invention must be shown in as complete detail as is contained in the patent claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). Clearly, here this is not the case.

On page 3 of paper number 4, the Examiner stated that as to claims 2, 5 and 22, Bassetti et

al. teaches the spread spectrum unit (74) being arranged between the graphic processing unit (72, 52, 54, 56, 60) and the LCD display transmitter (62) (see figure 7 and column 9). Unlike page 2 of paper number 4 concerning claim 1, the Examiner states that graphic processing unit only includes 72, 52, 54, 56, 60 and not 62 but that 62 is now the LCD display transmitter with respect to the rejection of claims 2, 5 and 22.

In the present invention, in claim 2, the LCD transmitter is for transmitting the image signal to the LCD, but reference 62 of Bassetti is the LCD controller and not the transmitter. Furthermore, even if 62 was the LCD transmitter, still reference 74 is not between the alleged graphic processor of 72, 52, 54, 56, 60 and the LCD 22. As seen in figure 7, the spread spectrum unit 74 is sending a signal to both reference 60 and 62 and reference 60 is sending a signal directly to 62. Therefore, technically, reference 74 is not between 60 and 62 because of the signal path seen in figure 7.

Furthermore, as mentioned in claim 2, Bassetti does not disclose the LCD transmitter *being installed on a clock signal line for transmitting the clock signal.* As seen in figure 7, the LCD controller is not transmitting the clock signal or at least such is not disclosed in Bassetti.

The Examiner stated that as to claims 12 and 14, Bassetti et al. teaches the step of modulating the frequency (74) being between the steps of converting the image signal(from first clock rate (MCLK to second clock rate VCLK) and the transmitting the image signal (62) (see figure 7 and column 9).

Concerning claims 12 and 14, the Examiner is now stating that the converting of the image signal is from the first clock rate MCLK to the second clock rate VCLK which is distinct from what

was mentioned earlier concerning the converting of image signal in the rejection of claim 1 (graphic unit being 72, 52, 54, 56, 60, 62) and also from the rejection of claim 2 (graphic unit being 72, 52, 54, 56, 60. Respectfully, there should at least be a consistency of what is being argued as the graphic processing unit throughout the office action.

As seen in Bassetti, the image signal from the first clock rate MCLK to second clock rate VCLK is not converted into a signal accommodating display of the image signal. As mentioned in col. 8, lines 52 to col. 9, line 33 of Bassetti, "the first clock synthesizer 70 is used to generate a memory clock MCLK, which is used to time and sequence accesses to video memory 50. Video memory 50 stores pixels for display on CRT 24 and LCD display 22. The image of the screen stored in graphics memory 50 can be stored either as raw pixels or as characters of text along with a character map for converting text to pixel bitmaps... Pixels are then clocked to RAM look-up table 56, which contains a table in memory to re-map the color represented by a pixel... Pixels from RAM look-up table 56 are also sent to LCD display 22 through a second connection to EMI FIFO 60. EMI FIFO 60 receives pixels from RAM look-up table 56. These pixels are written to EMI FIFO using video clock VCLK. The pixels are temporarily stored in EMI FIFO 60 and read out to LCD controller 62 using a *modulated video clock*, VCLK_SS. *LCD controller 62 performs formatting of pixels and gray-scale conversion so that the pixels are in a format accepted by LCD display 22.* The formatted pixels are clocked out of LCD controller 62 and to LCD display 22 over panel interface 80." (emphasis added).

Therefore, as seen above, the image signal is not in a format acceptable by an LCD display until LCD controller 62 has processed the signal and already the LCD has accepted the modulated

video clock VCLK_SS signal.

Therefore, if we assume that the LCD controller 62 is also for transmitting the signal to the LCD, then clearly one cannot say that the modulating step in Bassetti is between the converting and transmitting step because in Bassetti, the converting step is not completed until after the modulating step has already been completed and the signal is inputted into the controller which is still processing the signal accommodating a display of the image signal.

As mentioned above in MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Every element must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). Clearly, here since Bassetti does not disclose every element literally as arranged in claims 12 and 14, claims 12 and 14 are not anticipated.

II. REJECTION OF CLAIMS (35 U.S.C. § 103)

Claims 4 and 19-21 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Bassetti et al. (5,757,338) in view of Leung et al. (6,580,432). The Applicant respectfully traverses.

According to MPEP 706.02(j), the following establishes a *prima facie* case of obviousness under 35 U.S.C. §103:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Concerning the Examiner's burden of proving a *prima facie* case of obviousness, the Examiner has not fulfilled the third criteria of MPEP 706.02(j) of the prior art references teaching or suggesting all of the claim limitations.

The Examiner states that Bassetti et al. fails to point out the spread spectrum unit being integrally formed with either one of the graphic processing unit and a liquid crystal display transmitter. However, the Examiner goes on to state that Leung et al. teaches the spread spectrum unit (130) can be integrally formed with the graphic processing unit (see figure 1 and column 3, lines 27-36).

However, looking at col. 3, lines 27-36, Leung states that "The spread-spectrum clock signal

128 is generated by a jitter clock generator 130 that may be integrated as part of the spread-spectrum FIFO 106 or may be an external circuit, if desired." The passage is stating that the jitter clock generator 130 and the spread-spectrum FIFO 106 can be integrated and not the graphic processing unit and the spread spectrum unit. Furthermore, figure 1 of Leung clearly suggests the lack of such integration.

Further, in col. 3, lines 49-51, Leung states that "The jitter clock generator 130 serves as the spread spectrum clock generator and receives an amplitude control signal 140." Col. 4, line 4 to line 7 of Leung states "The spread-spectrum FIFO 106 in conjunction with the spread-spectrum clock generator 130 facilitates the passing of data and control signals from an unjittered domain to a jittered domain." Therefore, clearly, both 130 and 106 concern the spread spectrum unit and have nothing to do with processing the graphics. Therefore, all of the claim limitations are not taught or suggested as mandated to fulfill the Examiner's burden of proving *prima facie* case of obviousness according to MPEP 706.02(j).

Furthermore, according to the first criteria of MPEP 706.02(j), the Examiner has failed in his burden of showing a proper suggestion or motivation to modify or combine the references.

According to the Examiner, it would have been obvious to have modified Bassetti et al. with the teaching of Leung et al., so as to reduce the number of connection wires, ensure more stable connections and reduce amounts of hardware on its internal structure and interface.

The first point in MPEP 706.02(j) states that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill

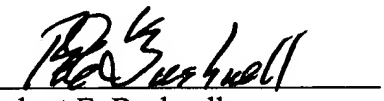
in the art, to modify the reference or to combine reference teachings. "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability. *In re Dembiczak*, 175 F.3d 994, 50 USPQ.2d 1614 (Fed. Cir. 1999). The showing must be "clear and particular" without broad generalized conclusory statements. *Id.* There must be specific statements showing the scope of the suggestion, teaching, or motivation to combine the prior art references. *Id.* at 1000. There must be an explanation to what specific understanding or technical principle would have suggested the combination of references. *Id.* The mere fact that the teachings of the prior art can be combined or modified does not itself make the resultant *prima facie* obvious. MPEP 2143.01.

Therefore, respectfully, here the Examiner's suggestion of the motivation being to reduce the number of connection wires, ensure more stable connections and reduce amounts of hardware on its internal structure and interface is not shown to be from the references themselves or shown to be known by one of ordinary skill. No passage was cited from the references and also a person of ordinary skill it art was not properly defined. Furthermore, respectfully, the motivation is improperly not "clear and particular" but a broad generalized conclusory statement. To simply state that integration is to reduce the number of connection wires is very broad and a conclusory statement. Furthermore, according to MPEP 706.02(j), "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." Therefore, the applicant's disclosure cannot be used to show the motivation to combine or modify the references.

In view of the foregoing amendments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. If there are any questions, the examiner is asked to contact the applicant's attorney.

No fee is incurred by this Response. Should there be a deficiency in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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